UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/432,819	11/02/1999	QUE-WON RHEE	10991663-1	1594

22878 7590 04/23/2002

AGILENT TECHNOLOGIES, INC.
INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT.
P.O. BOX 7599
M/S DL429
LOVELAND, CO 80537-0599

EXAMINER	
PARK, ILWOO	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 04/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/432,819	Applicant(s) RHEE, QUE-WON
	Examiner Ilwoo Park	Art Unit 2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-12* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-12 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities: the reference numerals of the phraseology "synchronization block 11" in page 5, lines 21-22, "translation block 12" in page 5, lines 24-25 and in page 6, lines 14-15, and "queue block 13" in page 6, line 18 should be in accordance with the fig. 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Chambers et al., US patent No. 6,108,738.

As to claim 1, Chambers et al teach on an integrated circuit [col. 10, lines 44-47], an interface block [bridge 480 in fig. 5: col. 9, lines 18-20] that provides an interface between an

internal bus [internal PCI bus 416] of the integrated circuit and a socket of a logic block [col. 10, lines 41-44], the interface block comprising:

a synchronization module that performs any needed synchronization [col. 9, lines 37-45] between a clock domain of the internal bus and a clock domain [external PCI bus 490] of the socket of the logic block;

a translation module that, for data transferred between the internal bus and the socket of the logic block, provides translation [col. 9, lines 37-45] of block encoding of the data;

a queue module, that buffers [col. 9, lines 37-45] data flowing between the internal bus and the socket of the logic block; and

a driver module [col. 8, line 59-col. 9, line 11] that handles low level and electrical drive specifications of the internal bus.

5. As to claim 2, Chambers et al teach the synchronization module can be implemented as one of:

a null synchronization block where no synchronization is required between the clock domain of the internal bus and the clock domain of the socket of the logic block;

a ratio synchronization block where the clock domain of the internal bus is related to the clock domain of the socket of the logic block by a fixed multiplier ratio; and

a full synchronization block [col. 9, lines 30-37] where there is no phase relationship between the clock domain of the internal bus and the clock domain of the socket of the logic block.

6. Claims 4 and 6-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Malladi, US patent No. 5,870,310.

As to claim 4, Malladi teaches a method for providing an interface [col. 2, lines 3-9] between an internal bus [CPU bus] of an integrated circuit [system-on-a-chip: col. 1, line 57-col. 2, line 3] and a socket of a logic block [e.g., memory shell 122, memory controller 322, or display controller unit 352 in figs. 1-3] within the integrated circuit, the method comprising the steps of:

a) performing any needed synchronization [timing requirements: col. 2, lines 3-9] between a clock domain [col. 3, lines 42-47] of the internal bus and a clock domain [col. 4, lines 43-48] of the socket of the logic block within a synchronization module;

b) performing any required translation [communication protocols: col. 2, lines 3-9] of block encoding of data transferred between the internal bus and the socket of the logic block using a translation module;

c) buffering data [col. 8, lines 61-66] flowing between the internal bus and the socket of the logic block using a queue module; and

d) handling [col. 4, line 65-col. 5, line 2] low level and electrical drive specifications of the internal bus using a driver module.

7. As to claim 6, Malladi teaches providing buffers between modules to allow pipelined operation [col. 8, lines 61-66].

8. As to claim 7, Malladi teaches on an integrated circuit [system-on-a-chip: col. 1, line 57-col. 2, line 3], an interface block [e.g., data processing shells 141a-141c, 141b', 301, 327, or 337 in figs. 1-3] that provides an interface [col. 2, lines 3-9] between an internal bus [CPU bus] of the integrated circuit and a socket of a logic block [e.g., memory shell 122, memory controller 322, or display controller unit 352 in figs. 1-3], the interface block comprising:

a plurality of modules [col. 2, lines 3-9] connected in series [e.g., Ref. Nos. 140a, 108, and 150a in fig. 1], where any needed synchronization [timing requirements: col. 2, lines 3-9] between a clock domain [col. 3, lines 42-47] of the internal bus and a clock domain [col. 4, lines 43-48] of the socket of the logic block, any required translation [communication protocols: col. 2, lines 3-9] of block encoding of data, any buffering of data [col. 8, lines 61-66] flowing between the internal bus and the socket of the logic block, and any low level and electrical drive specifications of the internal bus are performed by the plurality of modules so that one module from the plurality of modules performs [col. 2, lines 3-9] a single function.

9. As to claim 8, Malladi teaches a first module in the plurality of modules is a synchronization module that performs any needed synchronization [timing requirements: col. 2, lines 3-9] between the clock domain of the internal bus and the clock domain of the socket of the logic block within a synchronization module.

10. As to claim 9, Malladi teaches one module in the plurality of modules is a translation module [communication protocols: col. 2, lines 3-9] that, for data transferred between the internal bus and the socket of the logic block, provides translation of block encoding of the data.

11. As to claim 10, Malladi teaches one module in the plurality of modules is a queue module [col. 8, lines 61-66], that buffers data flowing between the internal bus and the socket of the logic block.

12. As to claim 11, Malladi teaches one module in the plurality of modules is a driver module that handles [col. 4, line 65-col. 5, line 2] low level and electrical drive specifications of the internal bus.

13. As to claim 12, Malladi teaches providing a plurality of buffers situated between modules in the plurality of modules, the buffers used to pipeline [col. 8, lines 61-66] the interface block.

Allowable Subject Matter

14. Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication should be directed to Ilwoo Park, whose telephone number is (703) 308-7811 or via e-mail, ***ilwoo.park@uspto.gov***. The Examiner can normally be reached Monday through Friday from 9:00 AM to 5:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jeffrey A. Gaffin, can be reached at (703) 308-3301.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (for formal communications intended for entry),

(703) 746-7238 (for after-final communications),

or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist)

Ilwoo Park

April 10, 2002